

MS-7120

Version 1A

INTEL (R) Brookdale-GV Chipset

Willamette/Northwood/533Prescott 478pin mPGA-B Processor Schematics

CPU: Willamette/Northwood/533Prescott mPGA-478B Processor

System Chipset:

INTEL Brookdale-GV GMCH + ICH4

On Board Chipset:

BIOS -- FWH

LPC Super I/O -- W83627HF-AW

Clock Generator -- CY28349

AC'97 Codec -- RealTek ALC650/655

Onboard Lan Chipset-- RealTek RTL8101L

Expansion Slots:

AGP2.0 SLOT * 1 (PCI-BUS)

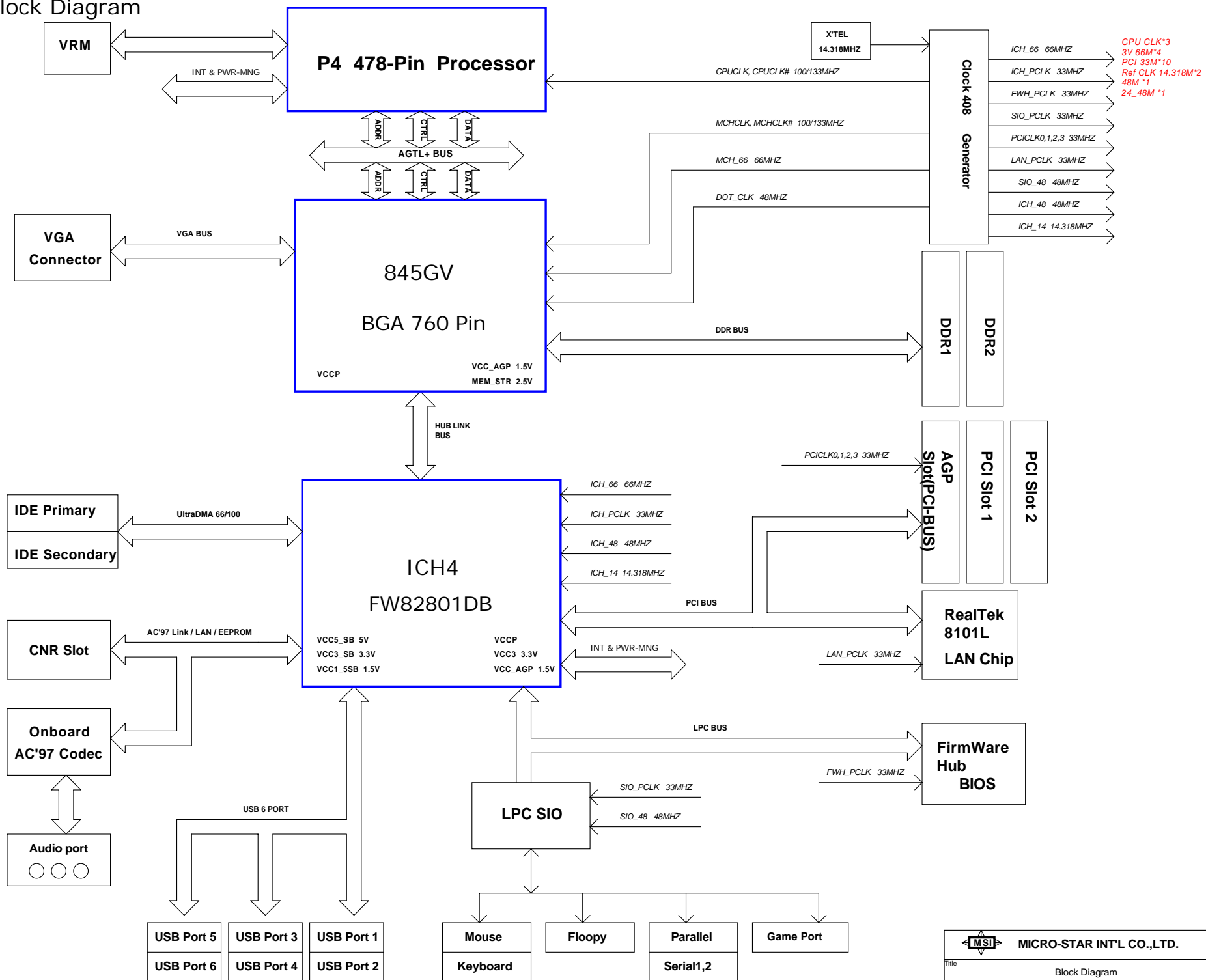
PCI2.2 SLOT * 2

Platform: Micro ATX

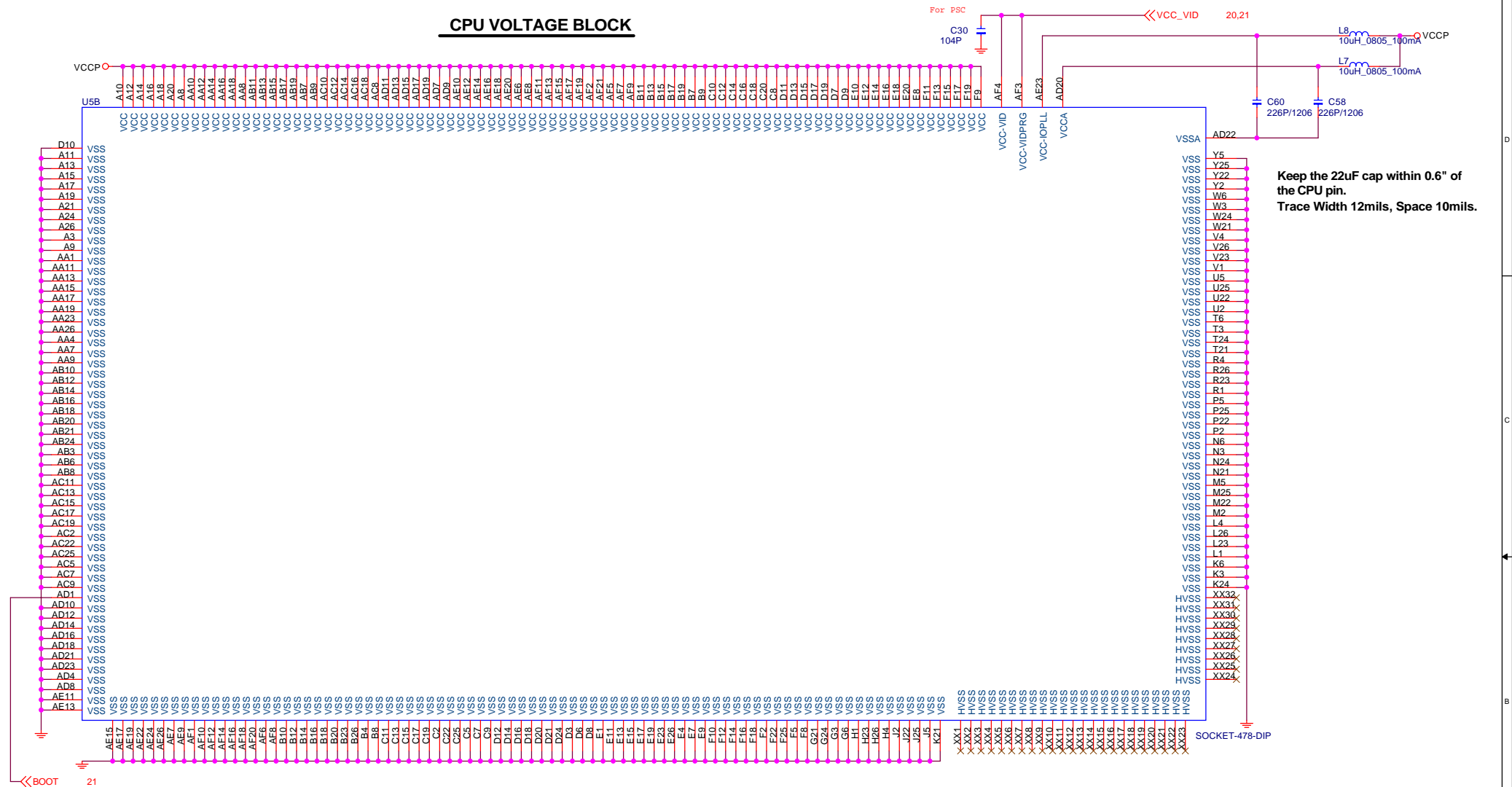
MODEL Config.	ORCAD Config.	Function	Option	ERP Number
MS7120-0A	cfig7120GV-LAN	GV+LAN+Com2	L	601-7120-A10
MS7120-100	cfig7120GV-LAN	GV+LAN+Com2	L	601-7120-010
MS7120-100	cfig7120GV-A	GV+LAN+Com2+Buzzer	A	601-7120-02S
MS7120-1A	cfig7120GV-LAN	GV+LAN+Com2+ESD	L	601-7120-???

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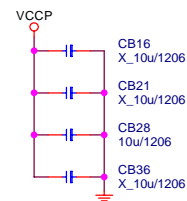
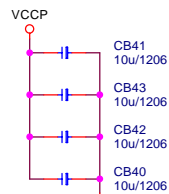
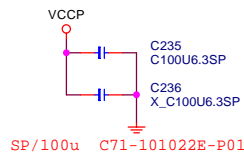
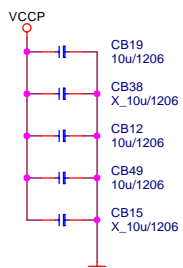
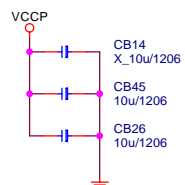
Block Diagram



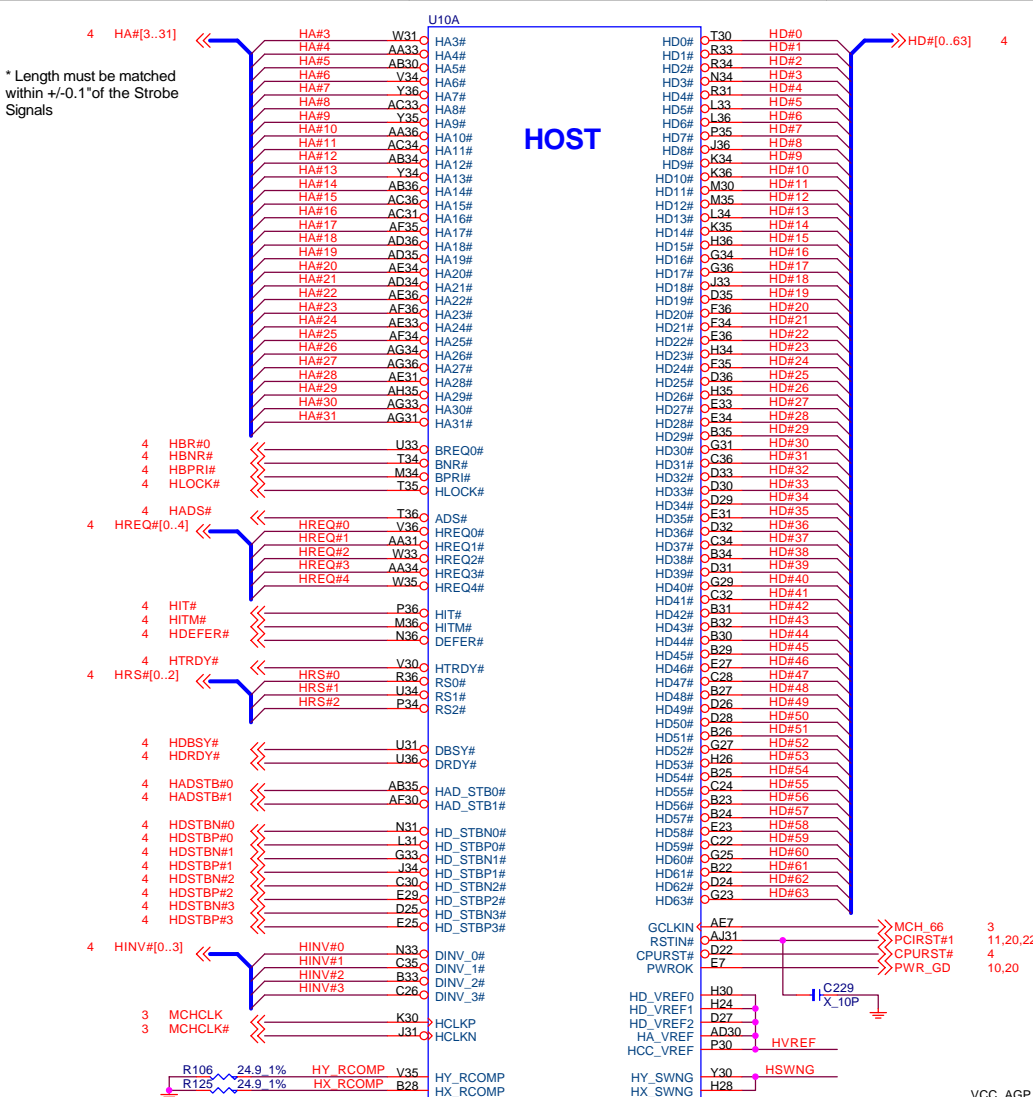
CPU VOLTAGE BLOCK



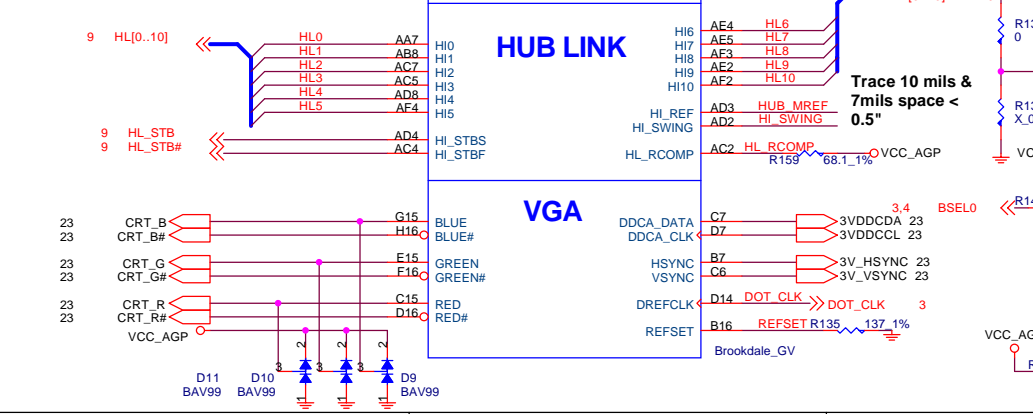
CPU DECOUPLING CAPACITORS



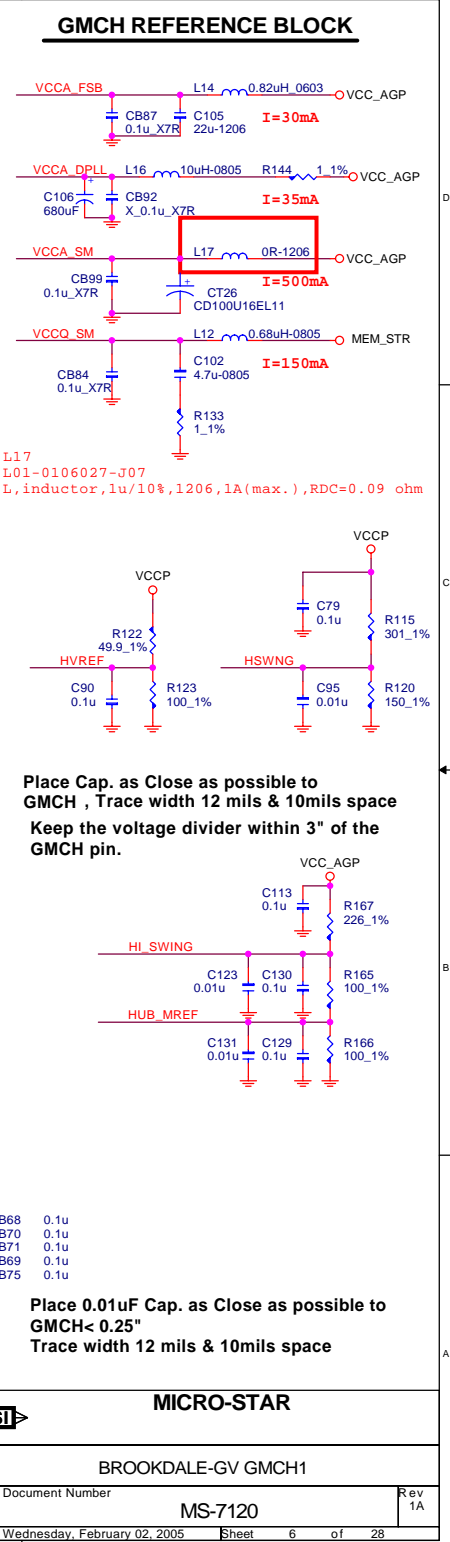
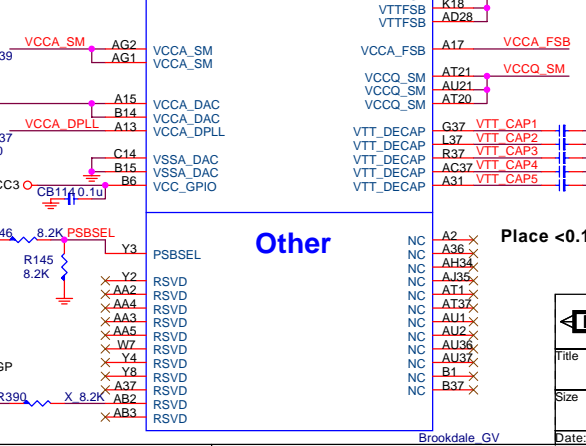
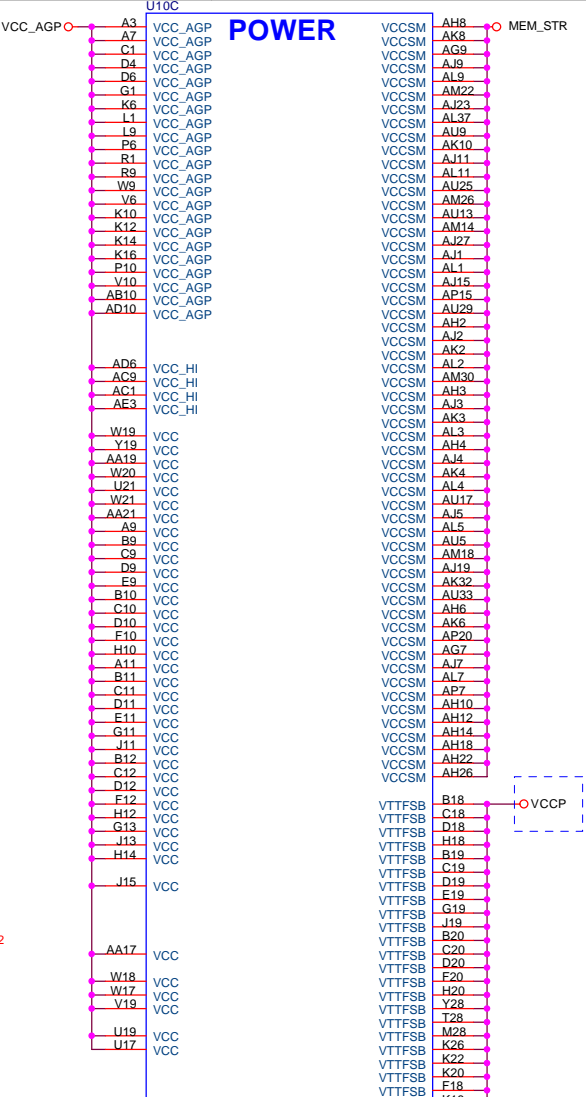
* Length must be matched within +/-0.1" of the Strobe Signals



Trace 10 mils & 7mils space < 0.5"



Trace 10 mils & 7mils space < 0.5"



Place Cap. as Close as possible to GMCH , Trace width 12 mils & 10mils space

Keep the voltage divider within 3" of the GMCH pin.

Place 0.01uF Cap. as Close as possible to GMCH< 0.25"

Trace width 12 mils & 10mils space



MICRO-STAR

Title			BROOKDALE-GV GMCH1		
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Rev		1A			

13,14 DDRMD[0..63] <<

U10B
DDRMD0 AN4 SDQ0
DDRMD1 AP2 SDQ1
DDRMD2 AT3 SDQ2
DDRMD3 AP5 SDQ3
DDRMD4 AN2 SDQ4
DDRMD5 AP3 SDQ5
DDRMD6 AR4 SDQ6
DDRMD7 AT5 SDQ7
DDRMD8 AT5 SDQ8
DDRMD9 AR6 SDQ9
DDRMD10 AT9 SDQ10
DDRMD11 AR10 SDQ11
DDRMD12 AT6 SDQ12
DDRMD13 AP6 SDQ13
DDRMD14 AT8 SDQ14
DDRMD15 AP8 SDQ15
DDRMD16 AP10 SDQ16
DDRMD17 AT11 SDQ17
DDRMD18 AT13 SDQ18
DDRMD19 AT14 SDQ19
DDRMD20 AT10 SDQ20
DDRMD21 AR12 SDQ21
DDRMD22 AR14 SDQ22
DDRMD23 AP14 SDQ23
DDRMD24 AT15 SDQ24
DDRMD25 AP16 SDQ25
DDRMD26 AT18 SDQ26
DDRMD27 AT19 SDQ27
DDRMD28 AR16 SDQ28
DDRMD29 AT18 SDQ29
DDRMD30 AP18 SDQ30
DDRMD31 AR20 SDQ31
DDRMD32 AR22 SDQ32
DDRMD33 AP22 SDQ33
DDRMD34 AP24 SDQ34
DDRMD35 AT26 SDQ35
DDRMD36 AT22 SDQ36
DDRMD37 AT23 SDQ37
DDRMD38 AT25 SDQ38
DDRMD39 AR26 SDQ39
DDRMD40 AP26 SDQ40
DDRMD41 AT28 SDQ41
DDRMD42 AR30 SDQ42
DDRMD43 AP30 SDQ43
DDRMD44 AT27 SDQ44
DDRMD45 AR28 SDQ45
DDRMD46 AT30 SDQ46
DDRMD47 AT31 SDQ47
DDRMD48 AR32 SDQ48
DDRMD49 AT32 SDQ49
DDRMD50 AR36 SDQ50
DDRMD51 AP36 SDQ51
DDRMD52 AP32 SDQ52
DDRMD53 AT33 SDQ53
DDRMD54 AP34 SDQ54
DDRMD55 AT35 SDQ55
DDRMD56 AN36 SDQ56
DDRMD57 AM36 SDQ57
DDRMD58 AK36 SDQ58
DDRMD59 AJ36 SDQ59
DDRMD60 AP36 SDQ60
DDRMD61 AM35 SDQ61
DDRMD62 AK35 SDQ62
DDRMD63 AK34 SDQ63

DDR

SMA0
SMA1
SMA2
SMA3
SMA4
SMA5
SMA6
SMA7
SMA8
SMA9
SMA10
SMA11
SMA12

AL25 DDRMAA0
AN25 DDRMAA1
AP23 DDRMAA2
AK20 DDRMAA3
AL19 DDRMAA4
AL17 DDRMAA5
AP19 DDRMAA6
AN17 DDRMAA7
AK16 DDRMAA8
AK26 DDRMAA9
AL15 DDRMAA10
AN15 DDRMAA11
AK15 DDRMAA12

>>DDRMAA[0..12] 13,14

SMAB1
SMAB2
SMAB4
SMAB5

AP25 DDRMAB1
AK23 DDRMAB2
AN19 DDRMAB3
AK18 DDRMAB4
AK18 DDRMAB5

>>DDRMAB1 13,14
>>DDRMAB2 13,14
>>DDRMAB3 13,14
>>DDRMAB4 13,14
>>DDRMAB5 13,14

SDQS0
SDQS1
SDQS2
SDQS3
SDQS4
SDQS5
SDQS6
SDQS7

AR2 SDQS0
AT7 SDQS1
AT12 SDQS2
AT17 SDQS3
AR24 SDQS4
AT29 SDQS5
AT34 SDQS6
AL36 SDQS7

>>SDQS[0..7] 13,14

SDM0
SDM1
SDM2
SDM3
SDM4
SDM5
SDM6
SDM7

AP4 SDM0
AR8 SDM1
AP12 SDM2
AR18 SDM3
AT24 SDM4
AP28 SDM5
AR34 SDM6
AL34 SDM7

>>SDM0 13,14
>>SDM1 13,14
>>SDM2 13,14
>>SDM3 13,14
>>SDM4 13,14
>>SDM5 13,14
>>SDM6 13,14
>>SDM7 13,14

SCKE0
SCKE1
SCKE2
SCKE3

AP13 MSCKE0
AN13 MSCKE1
AK14 MSCKE2
AL13 MSCKE3

>>MSCKE[0..3] 13,14

SCS0#
SCS1#
SCS2#
SCS3#

AL29 MSCS0#
AP21 MSCS1#
AK30 MSCS2#
AN31 MSCS3#

>>MSCS0# 13,14
>>MSCS1# 13,14
>>MSCS2# 13,14
>>MSCS3# 13,14

SCMDCLK_0
SCMDCLK_0#
SCMDCLK_1
SCMDCLK_1#
SCMDCLK_1#
SCMDCLK_2
SCMDCLK_2#
SCMDCLK_2#
SCMDCLK_3
SCMDCLK_3#
SCMDCLK_3#
SCMDCLK_4
SCMDCLK_4#
SCMDCLK_4#
SCMDCLK_5
SCMDCLK_5#
SCMDCLK_5#

AL21 DCLK0
AK22 DCLK0#
AN11 DCLK1
AP11 DCLK1#
AK34 DCLK2
AL33 DCLK2#
AP21 DCLK3
AN21 DCLK3#
AP9 DCLK4
AN9 DCLK4#
AP33 DCLK5
AN34 DCLK5#

>>DCLK0 13
>>DCLK0# 13
>>DCLK1 13
>>DCLK1# 13
>>DCLK2 13
>>DCLK2# 13
>>DCLK3 13
>>DCLK3# 13
>>DCLK4 13
>>DCLK4# 13
>>DCLK5 13
>>DCLK5# 13

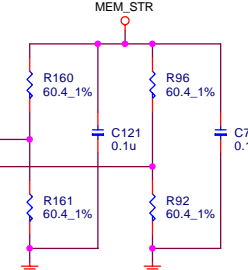
SBA_0
SBA_1
SRAS#
SCAS#
SWE#

AN27 MSBS0
AP27 MSBS1
AK28 MRAS#
AN29 MCAS#
AP29 MWE#

>>MSBS0 13,14
>>MSBS1 13,14
>>MRAS# 13,14
>>MCAS# 13,14
>>MWE# 13,14

SMX_RCOMP0
SMY_RCOMP

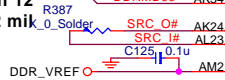
AF10 SMX_RCOMP
AJ34 SMY_RCOMP



Trace width 12 mil
with 10 mil space.
Place 0.1uF <1" to GMCH

Trace length
must as short
as possible
for SRCVEN

Trace width 12
mil with 12 mil
space for
SM_VREF.



SRCVEN_OUT#
SRCVEN_IN#
SM_VREF

AGP

V4 G_AD0
V2 G_AD1
V4 G_AD2
V5 G_AD3
U5 G_AD4
U4 G_AD5
U2 G_AD6
V3 G_AD7
T2 G_AD8
T3 G_AD9
T4 G_AD10
R2 G_AD11
R5 G_AD12
R7 G_AD13
T8 G_AD14
P3 G_AD15
P8 G_AD16
K4 G_AD17
K2 G_AD18
J2 G_AD19
M3 G_AD20
L5 G_AD21
L4 G_AD22
H4 G_AD23
G2 G_AD24
K3 G_AD25
J4 G_AD26
J5 G_AD27
J7 G_AD28
H3 G_AD29
K8 G_AD30
G4 G_AD31

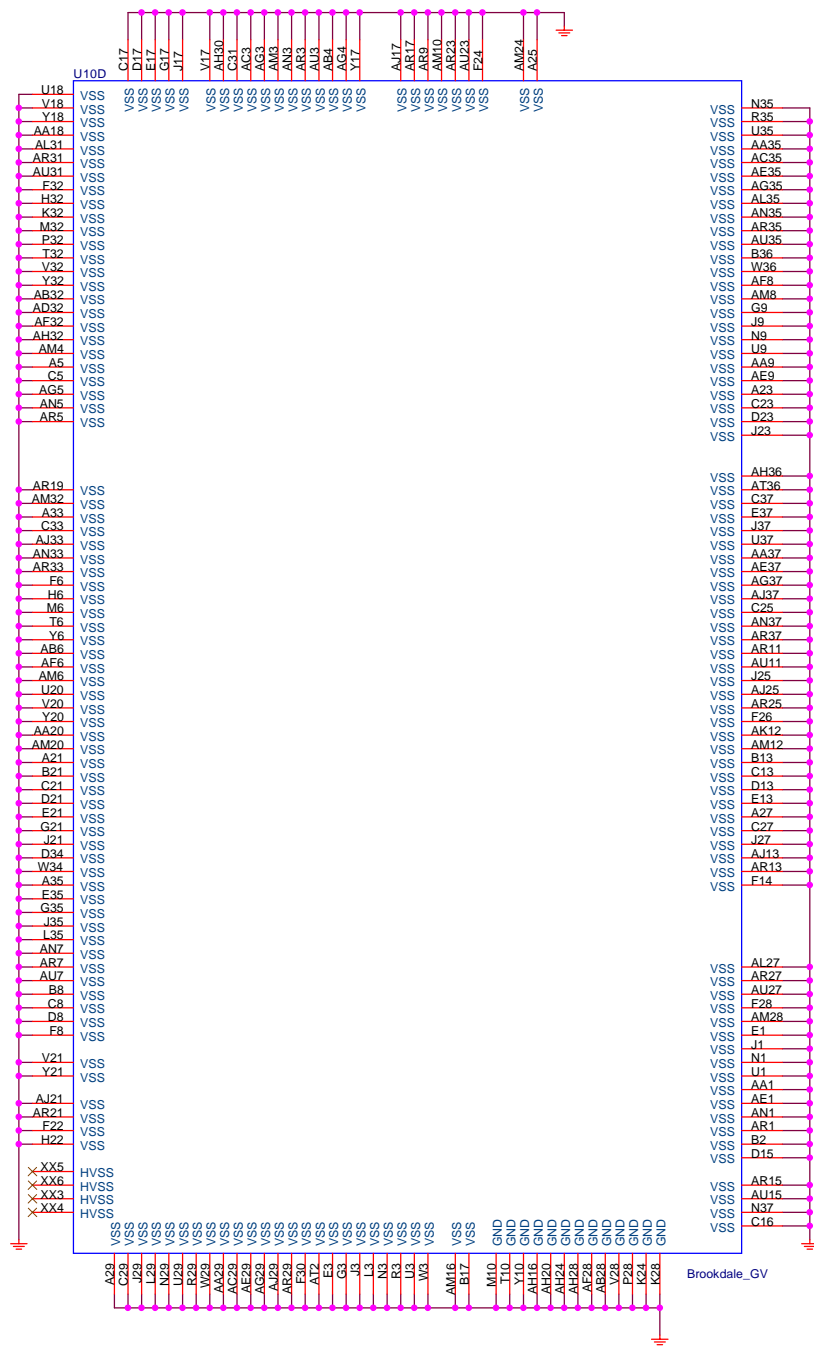
G_FRAME#
G_IRDY#
G_TRDY#
G_DEVSEL#
G_STOP#
G_PAR#
G_REQ#
G_GNT#
SBA0 C2
SBA1 D3
SBA2 D2
SBA3 E4
SBA4 E2
SBA5 F3
SBA6 F2
SBA7 F2
SB_STB#
SB_STB#
ST0 B4
ST1 B3
ST2 B3
AD_STB0 V8
AD_STB0# U7
AD_STB1 M8
AD_STB1# L7
PIPE# H8
RBF# G7
WBF# G5

AGP_VREF
AGP_RCOMP

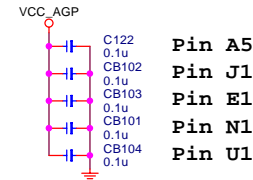
M4
N7
N5
N2
P2
P4
D5
B5
C3
D3
D2
E4
E2
F3
F2
F4
E5
C4
B4
B3
V8
U7
M8
L7
H8
G7
G5
W2
L2

Brookdale_GV

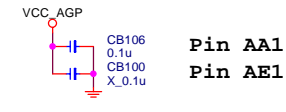
MSI		MICRO-STAR	
Title			
BROOKDALE-GV GMCH2			
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MS-7120			
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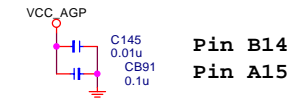
GMCH DECOUPLING CAPACITOR



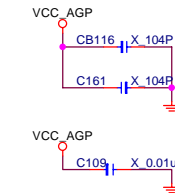
Place decoupling cap close to GMCH AGP Interface < 0.1"



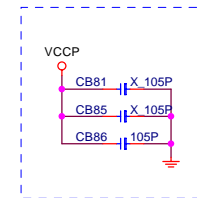
Place decoupling cap close to GMCH Hub-Link Interface < 0.1"



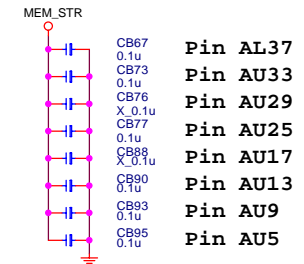
Place decoupling cap close to GMCH DAC Interface < 0.1"



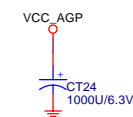
Place decoupling cap close to GMCH Core Logic Interface < 0.1"



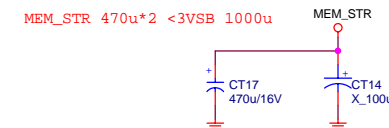
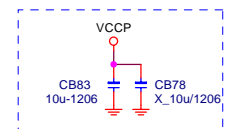
Place decoupling cap close to GMCH CPU Interface < 250mil in the Vtt corridor



Place decoupling cap close to GMCH Memory Interface < 0.1", with 18 mil track width



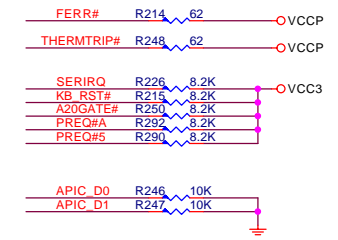
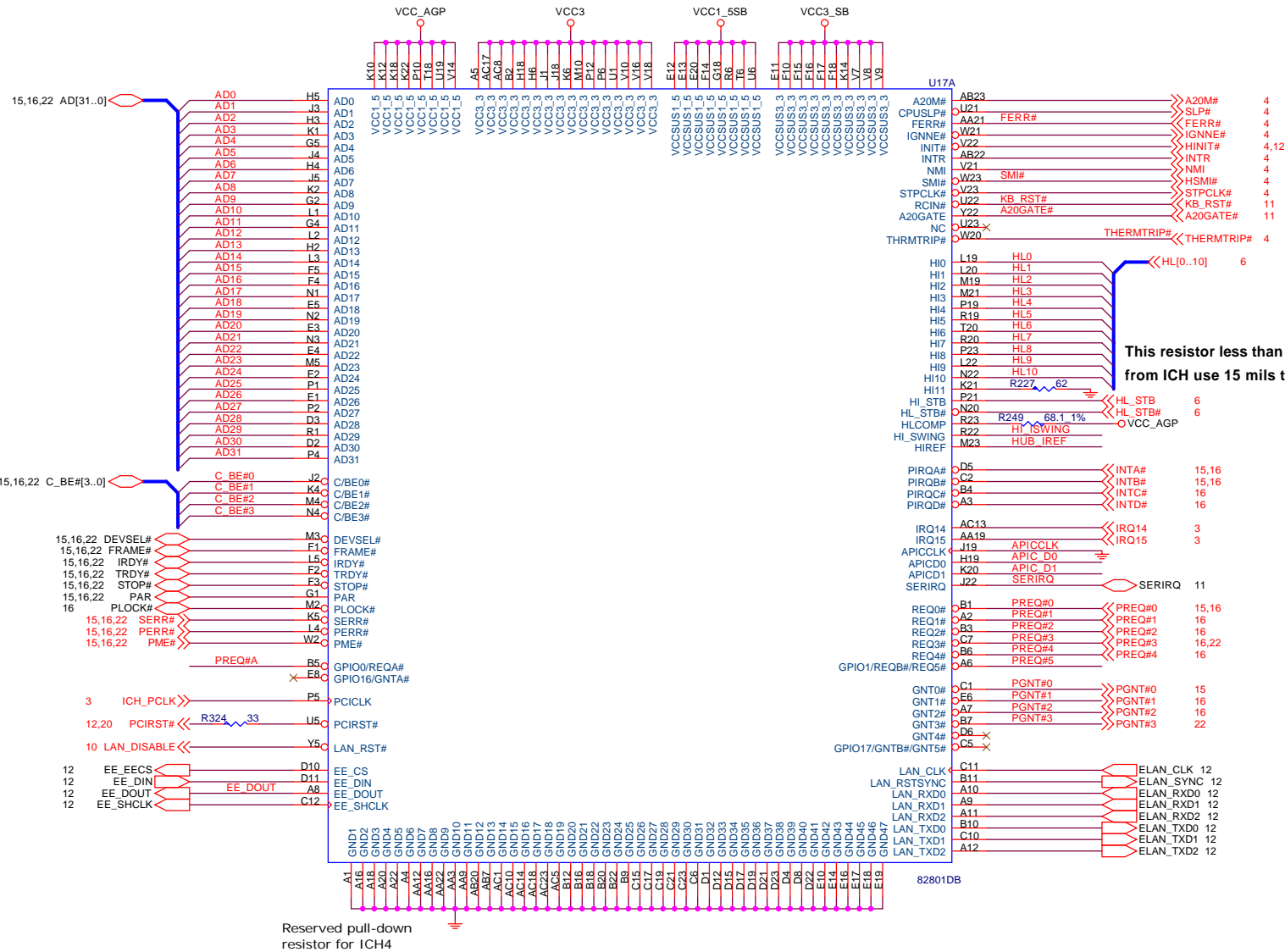
Place Bulk cap for Core Logic, AGP & Hub Link Interface



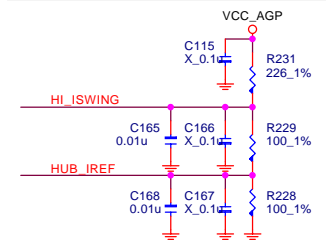
Place Bulk cap between GMCH & DIMM slot

ICH4 PCI / HUB LINK / CPU / LAN / INTERRUPT SIGNALS

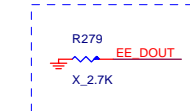
ICH4 PULL-UP/DOWN RESISTORS



ICH4 REFERENCE VOLTAGE

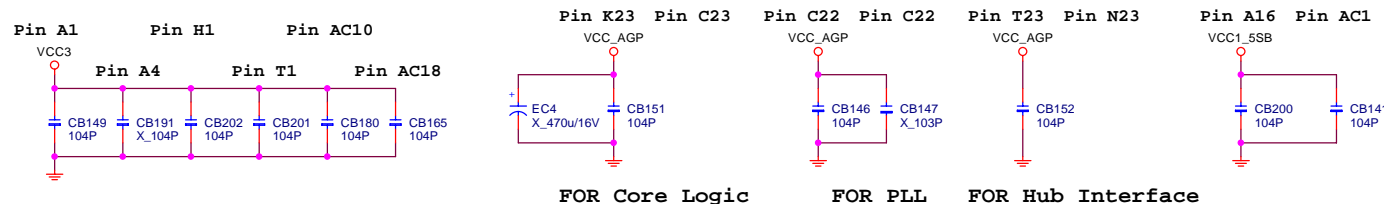


Place Cap. as Close as possible to ICH4 < 0.25"
Trace width use 12 mils and 10mils space



ICH4 DECOUPLING CAPACITORS

Place one 0.1u close to ICH4 <100 mil



FOR Core Logic

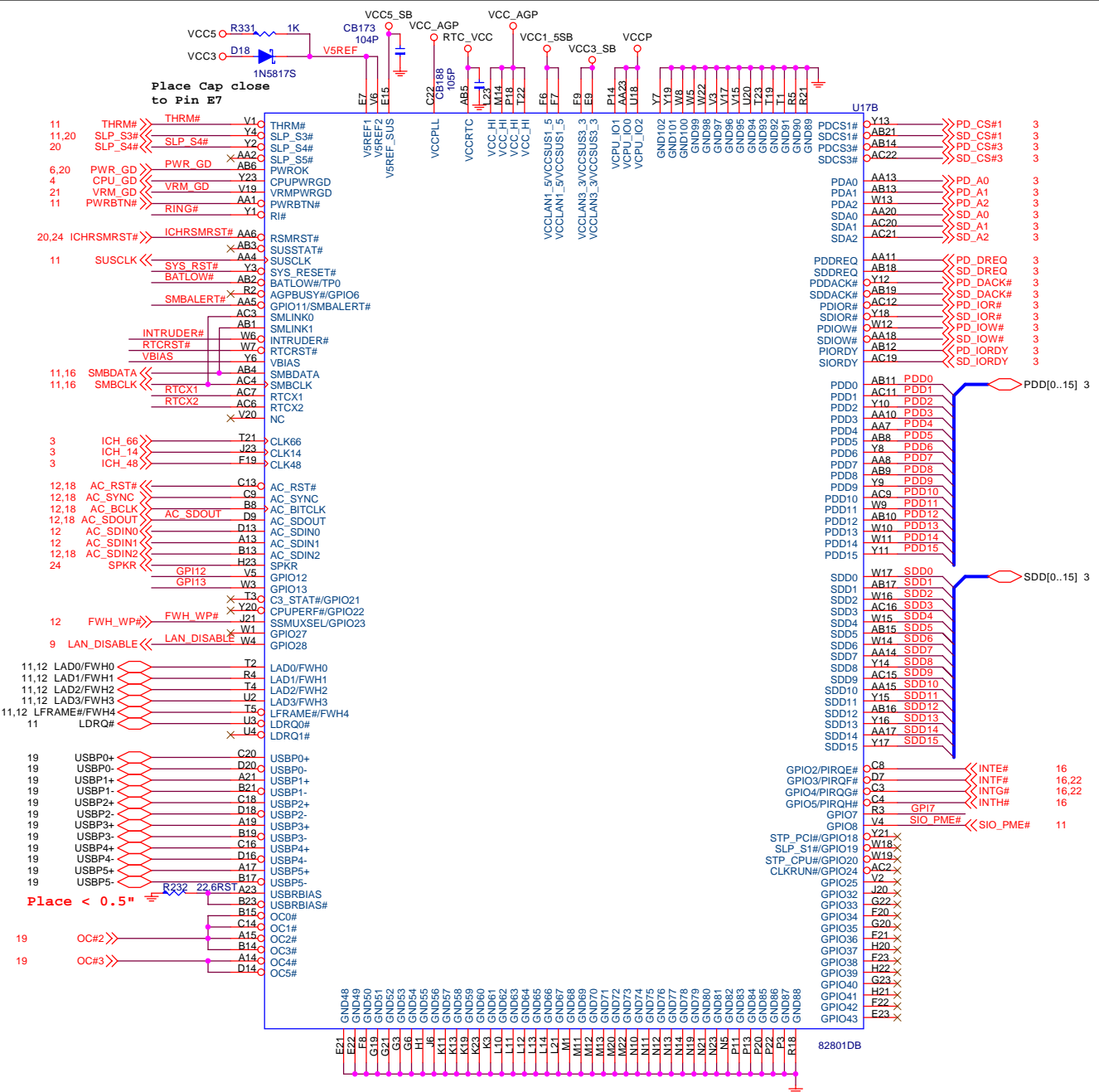
FOR PLL

FOR Hub Interface

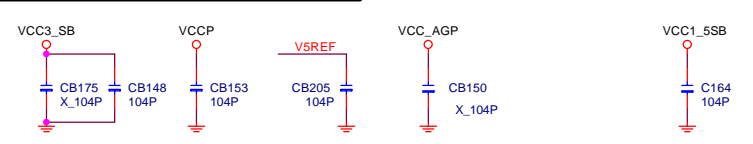


MICRO-STAR

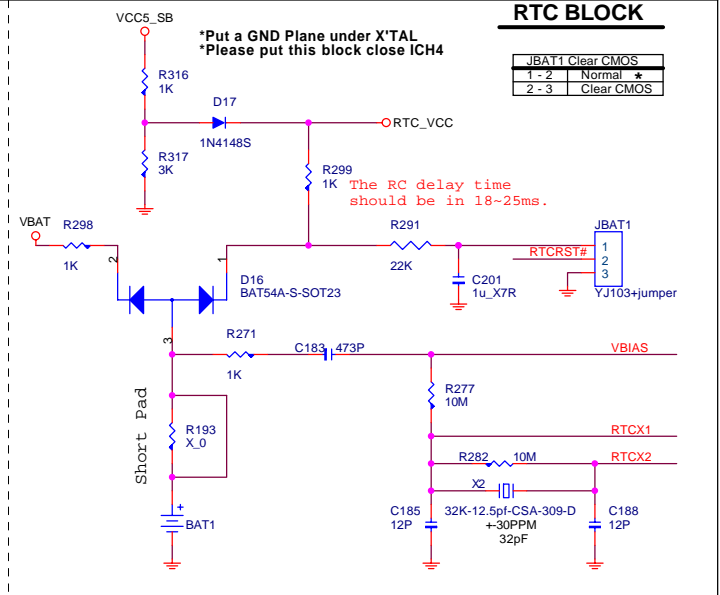
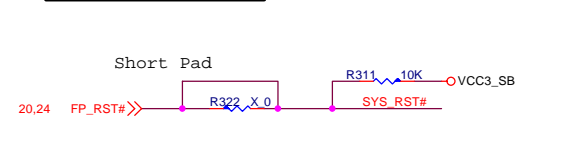
Title			
ICH4 PCI/H/LAN			
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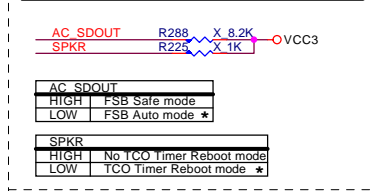
ICH4 DECOUPLING CAPACITOR



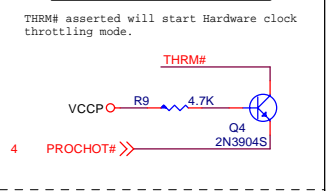
SYSTEM RESET



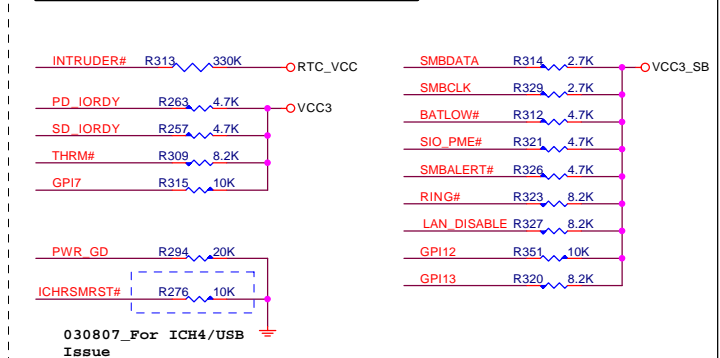
ICH4 STRAPPING RESISTORS



PROCHOT BLOCK



ICH4 PULL-UP/DOWN RESISTORS



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Title		
ICH4 OTHER		
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Pin 12

Pin connections (Left side):

- 1: LRESET#
- 2: LCLK
- 3: SERIRQ
- 4: LDRQ#
- 5: LFRAME#
- 6: LAD0
- 7: LAD1
- 8: LAD2
- 9: LAD3
- 10: GPX2/P15/GP14
- 11: GPY1/GP15
- 12: GPSA1/P12/GP10
- 13: GPSA2/GP17
- 14: GPX1/P14/GP12
- 15: GPY2/P16/GP14
- 16: GPSB1/P13/GP11
- 17: GPSB2/GP16
- 18: MSO/IRQIN0
- 19: MSI/GP20
- 20: VREF
- 21: VTI#3
- 22: VTI#2
- 23: VTI#1
- 24: AGND
- 25: -5VIN
- 26: -12VIN
- 27: +12VIN
- 28: AVCC
- 29: +3.3VIN
- 30: VCOREB
- 31: VCOREA
- 32: VID4
- 33: VID3
- 34: VID2
- 35: VID1
- 36: VID0
- 37: FANPWM1
- 38: FANIO1
- 39: FANPWM2
- 40: FANIO2
- 41: FANIO3
- 42: OVT#
- 43: BEEP
- 44: CASEOPEN#
- 45: PME#
- 46: WDTO/GP24
- 47: SDA/GP22
- 48: SCL/GP21
- 49: PSOUT#
- 50: PSIN
- 51: SUSLED/GP35
- 52: PLED/GP23
- 53: PWRCTL#/GP31
- 54: SUSCLIN/GP30
- 55: CLKIN
- 56: VSB
- 57: VBAT
- 58: VCC3
- 59: VCC_1
- 60: VCC_2
- 61: VCC_3
- 62: VCC_4

Pin connections (Right side):

- 1: DRVDEN0
- 2: DRVDEN1
- 3: INDEX#
- 4: MOA#
- 5: DSB#
- 6: DSA#
- 7: MOB#
- 8: DIR#
- 9: STEP#
- 10: WRDATA#
- 11: WE#
- 12: TRACK0#
- 13: WP#
- 14: RDATA#
- 15: HEAD#
- 16: DSKCHG#
- 17: LP D0
- 18: LP D1
- 19: LP D2
- 20: LP D3
- 21: LP D4
- 22: LP D5
- 23: LP D6
- 24: LP D7
- 25: LP_D[0..7]
- 26: LP_SLCT
- 27: LP_PE
- 28: LP_BUSY
- 29: LP_ACK#
- 30: LP_SLIN#
- 31: LP_INIT#
- 32: LP_ERR#
- 33: LP_AFD#
- 34: LP_STB#
- 35: IRRX/GP25
- 36: CIRRX/GP34
- 37: IRTX/GP26
- 38: SUSCLIN
- 39: DCDA#
- 40: DSRA#
- 41: SINA
- 42: RTSA#
- 43: SOUTA
- 44: CTS#
- 45: DTRA#
- 46: RIA#
- 47: DCDB#
- 48: DSRB#
- 49: SINB
- 50: RTSB#
- 51: SOUTB
- 52: CTSB#
- 53: DTRB#
- 54: RIB#
- 55: A20GATE#
- 56: KB_RST#
- 57: KBDATA
- 58: KBCLK
- 59: MSDATA
- 60: MSCLK
- 61: KBLOCK#
- 62: RSMRST#/GP33
- 63: PWROK/GP32
- 64: VSS1
- 65: VSS2
- 66: VSS3
- 67: VSS4

Pin connections (Bottom):

- 117: GND

[illegible][illegible]

VCC5 ○ R156 4.7K SOUTA

VCC5 ○ R173 X 4.7K SOUTB

○ R170 4.7K

VCC5 ○ R157 X 4.7K RTSA#

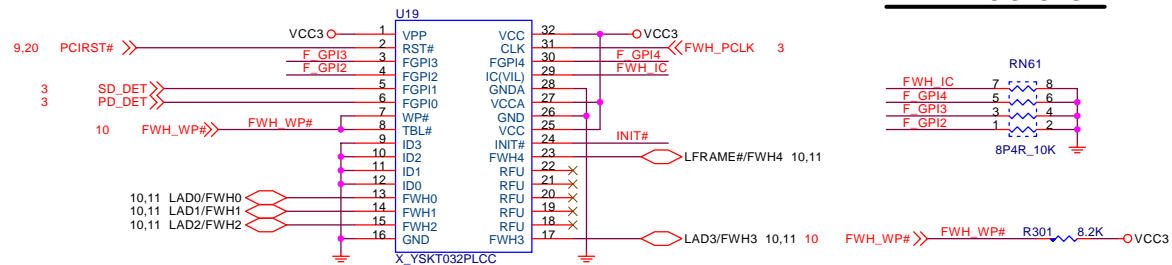
SOUTA	L: Disable KBC	H: Enable KBC
SOUTB	L: 24MHZ	H: 48MHZ
RTSA#	L: CFAD=2E	H: CFAD=4E
DTRA#	L: PNP Default	H: PNP no Default



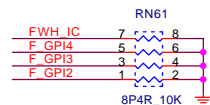
LPC SUPER I/O

Title				LPC SUPER I/O			
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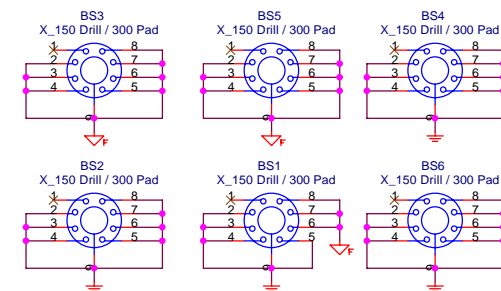
Firmware Hub (FWH)



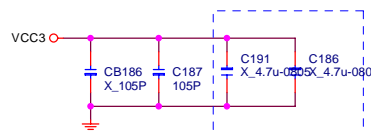
FWH RESISTORS



PCB Mounting Holes



FWH DECOUPLING CAPACITORS

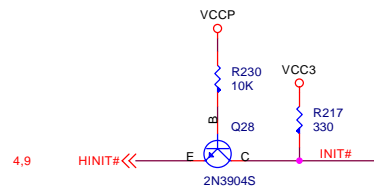


Place Cap. as Close to
FWH < 350 mil

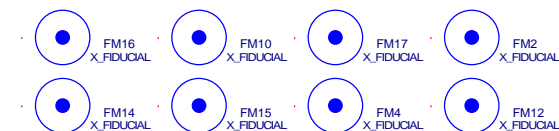
FWH write protect

BIOS_WP BIOS Update	
SHORT	Flash Write Disable
OPEN	Flash Write Enable (Default)

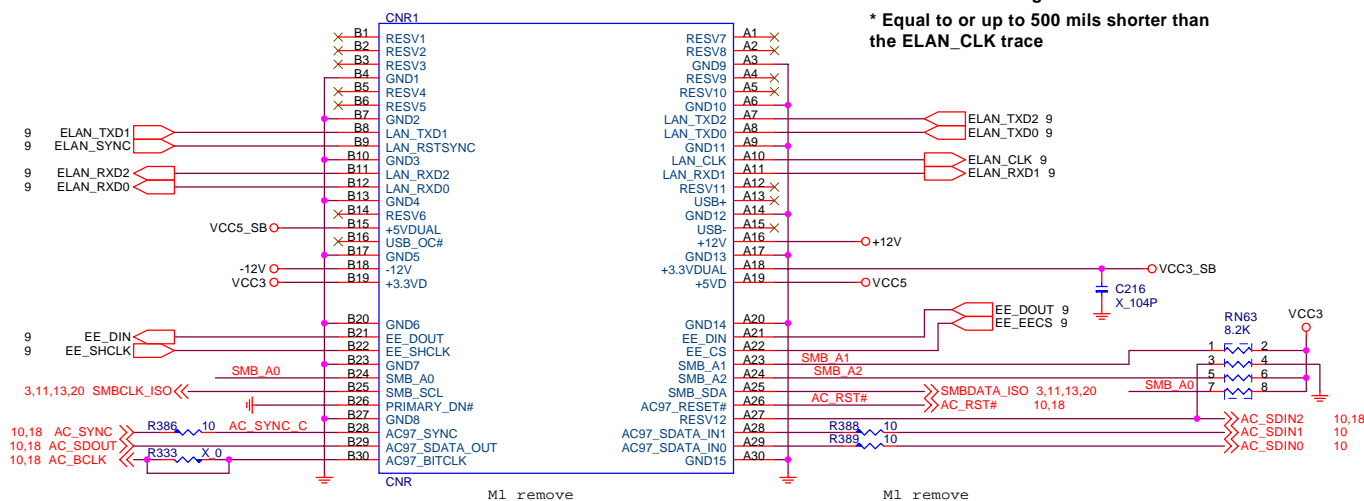
FWH INIT Signal Voltage Translation Block



PCB Fiducials

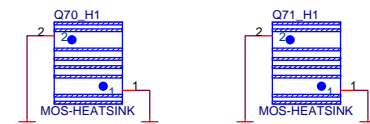


SIMULATION TRACE

**CNR RISER**

- * LAN Trace width : 5 mils
- * AC'97 Trace Spacing : 10 mils
- * Maxium trace length < 9.5"
- * Equal to or up to 500 mils shorter than the ELAN CLK trace

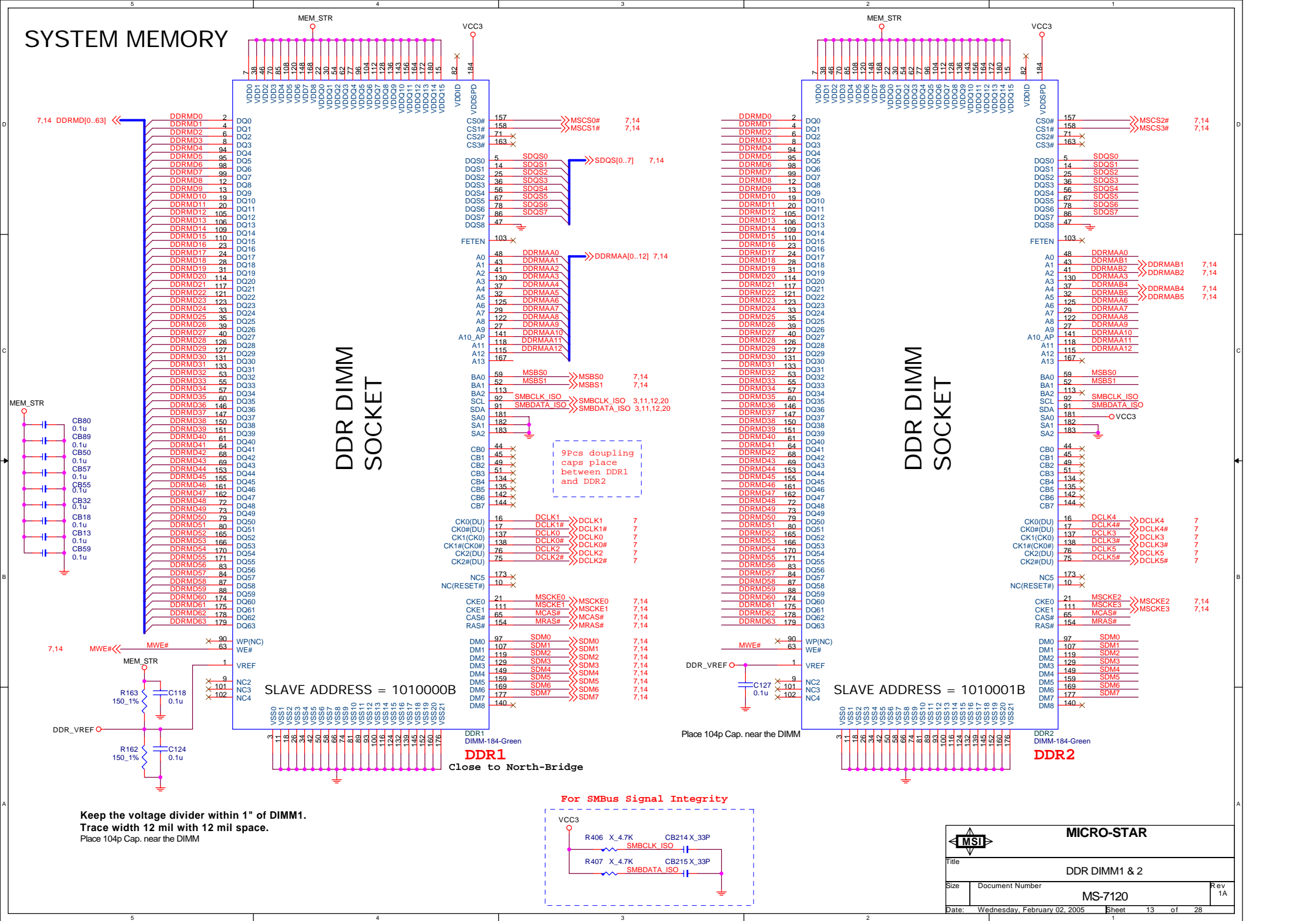
MOSFET HEATSINK



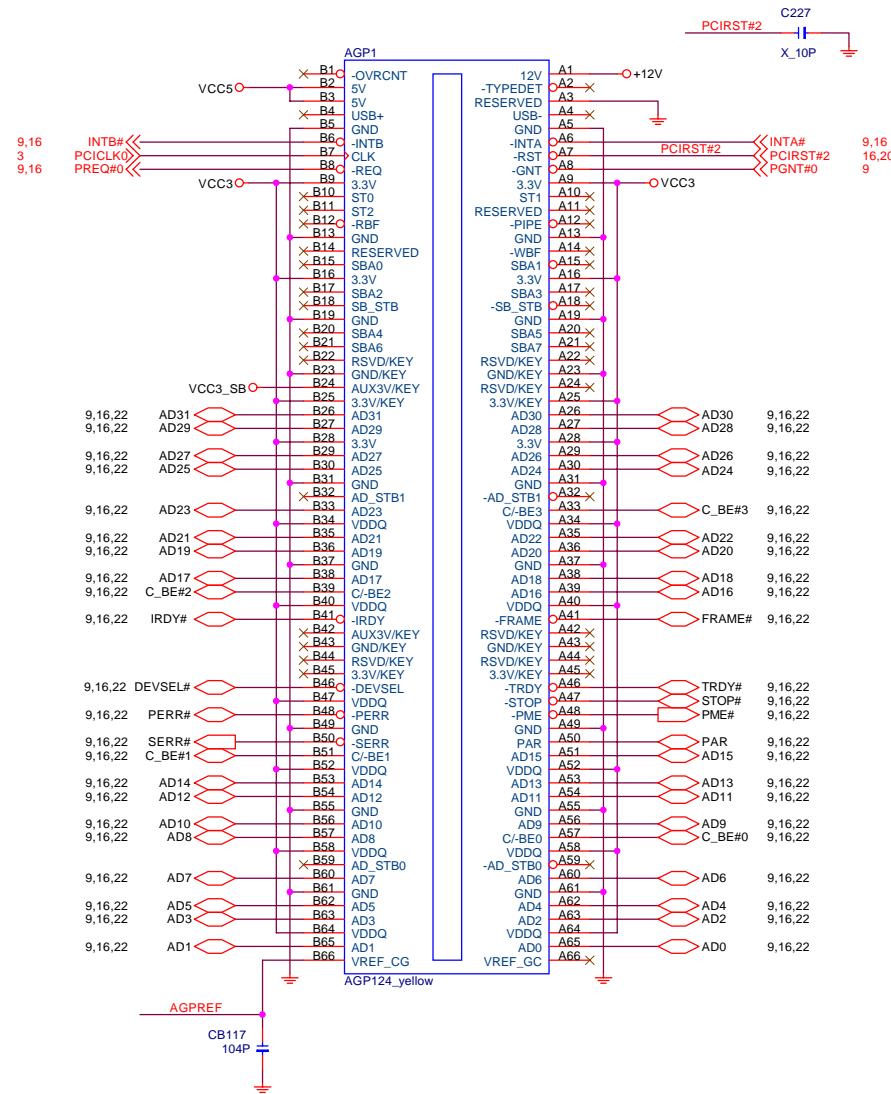
MICRO-STAR

Title			
FWH & CNR & Manual Part			
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SYSTEM MEMORY

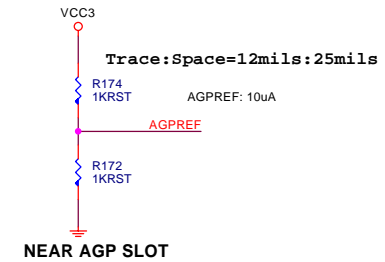


AGP UNIVERSAL 2X/4X SLOT

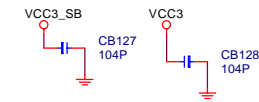


MASTER = PREQ0
INTA#

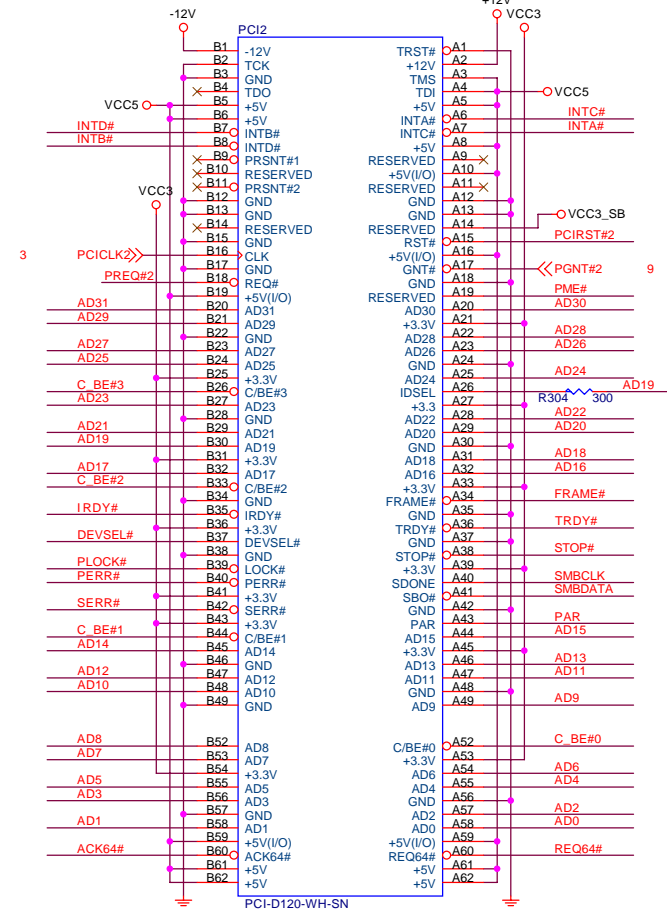
AGP SIGNAL REFERENCE CIRCUIT



AGP SLOT DECOUPLING CAPACITORS



PCI SLOT 2 (PCI VER: 2.2 COMPLY)

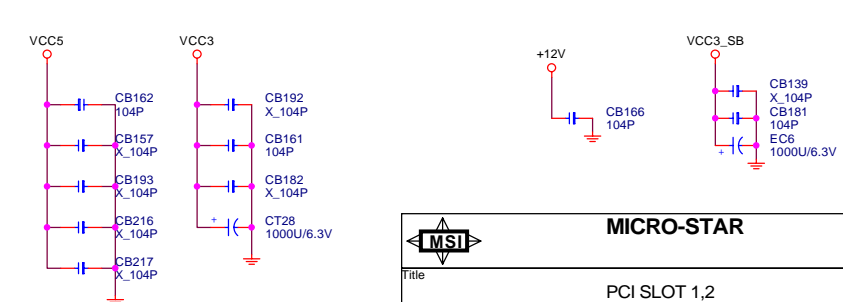


```

IDSEL = AD19
MASTER = PREQ2
INTC#

```

PCI SLOT DECOUPLING CAPACITORS



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SERIAL PORT 1



FLOPPY CONNECTOR



PS2 KEYBOARD & MOUSE CONNECTOR



PARALLAL PORT

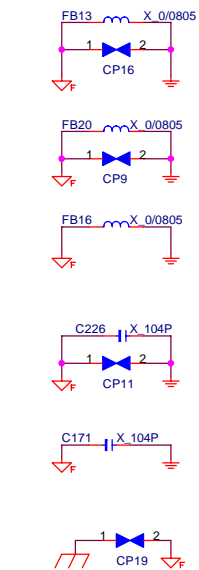
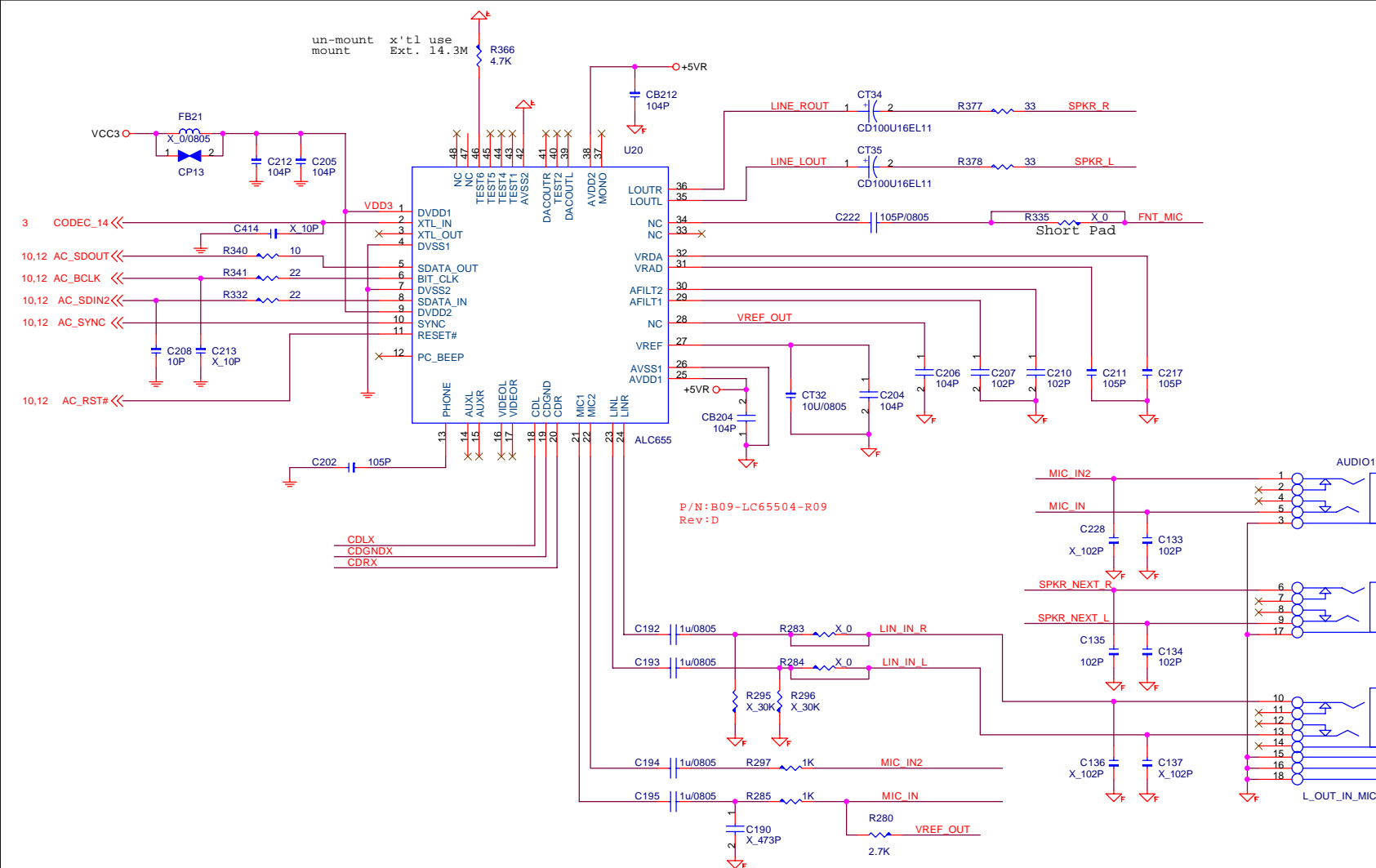


MICRO-STAR

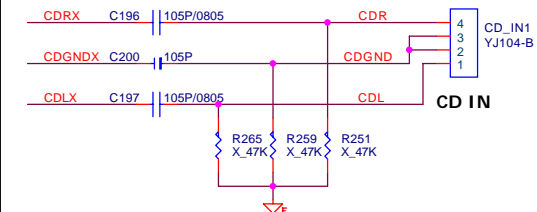
I/O CONNECTORS

MS-712C

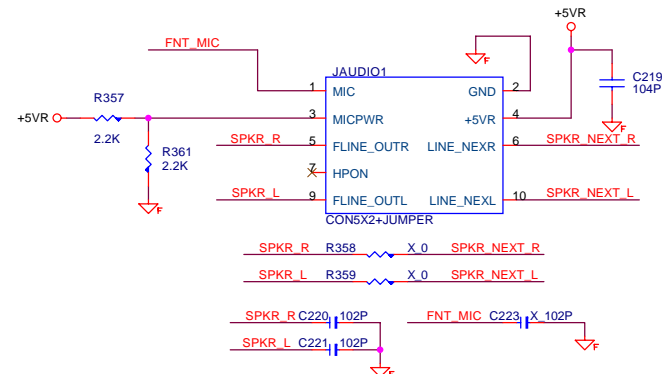
Date: Wednesday, February 02, 2005 Sheet 17 of 28



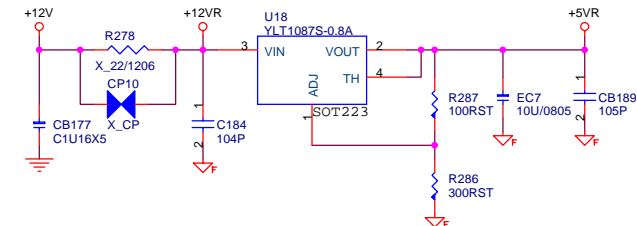
AUDIO CODE CD / AUX / MODEM IN HEADERS



FOR Intel INTERNAL HEADER



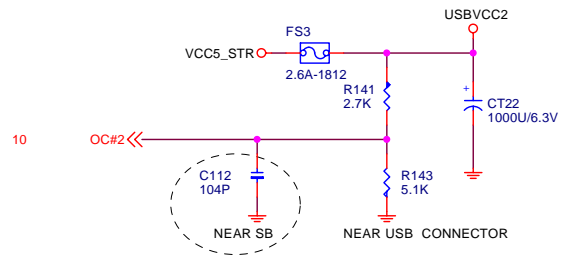
AUDIO CODE REGULATORS



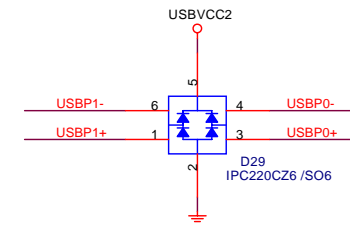
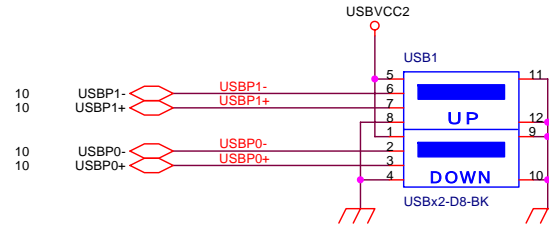
MICRO-STAR INT'L CO.,LTD.

Title			AC97 CODEC
Size	Document Number	MS-7120	Rev 1A
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POWER CIRCUIT FOR USB PORT 0~3

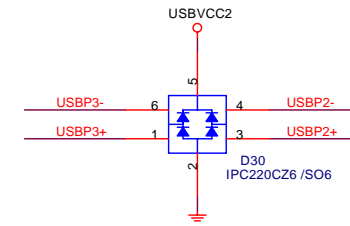
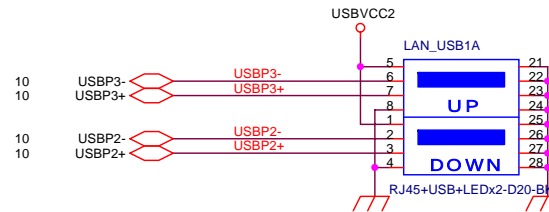


REAR PANEL USB CONNECTOR FOR USB PORT 0,1



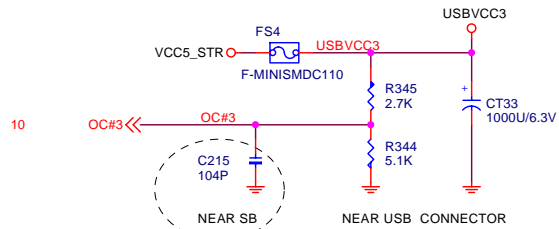
NEAR USB CONNECTOR

REAR PANEL USB CONNECTOR FOR USB PORT 2,3

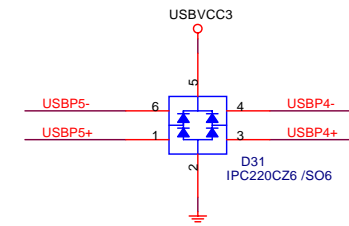
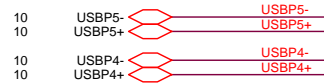


NEAR USB CONNECTOR

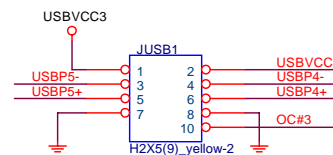
POWER CIRCUIT FOR USB PORT 4,5



FRONT PANEL USB CONNECTOR FOR USB PORT 4,5



NEAR USB CONNECTOR



Intel Front USB Header

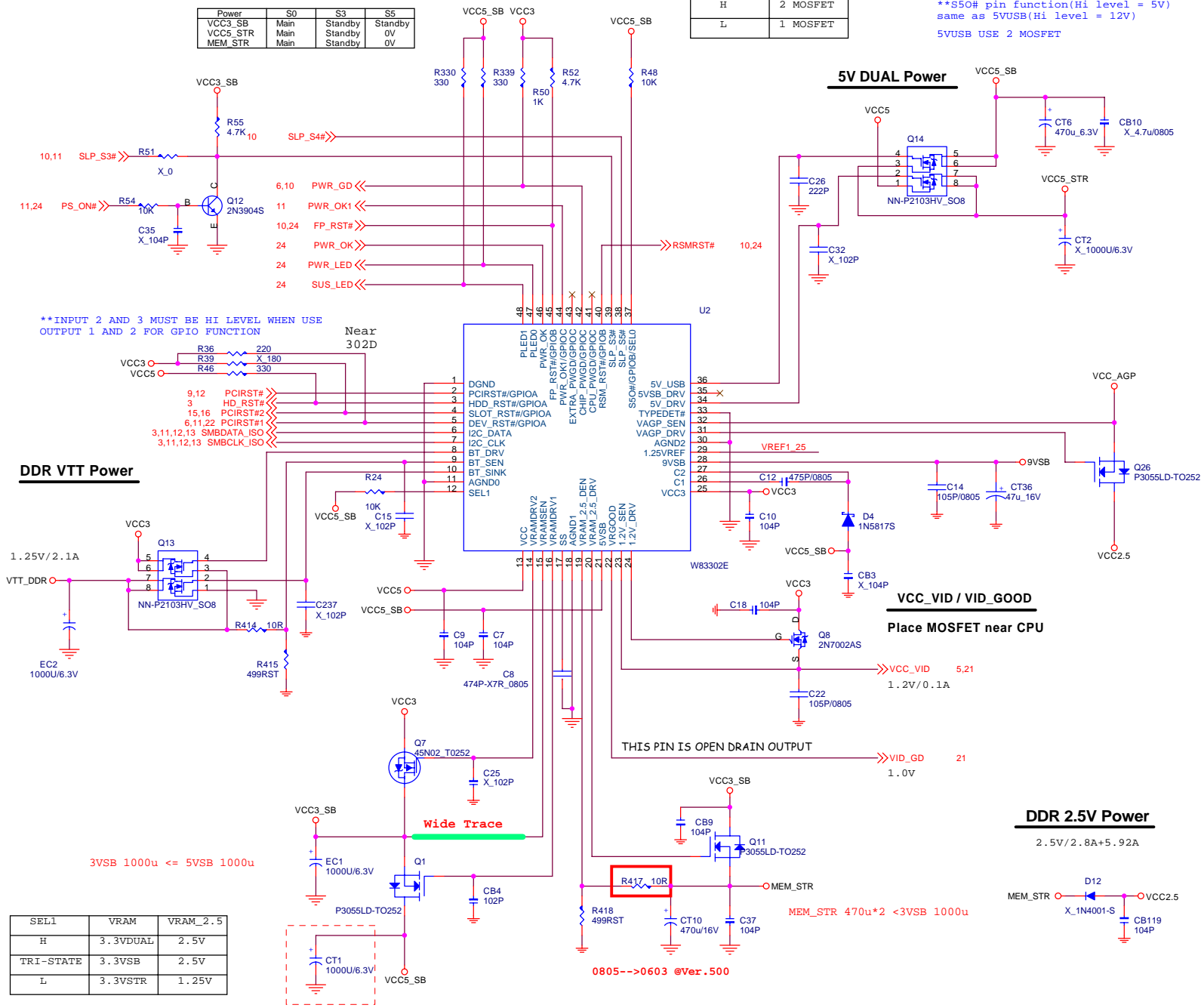
- * USB Trace width : 7.5 mils
- * USB Trace Spacing : 20 mils
- * Differential USB Signlas Trace, Spacing : 7.5 mils
- * USB Power Trace must be 50mils width

		MICRO-STAR	
Title: USB CONNECTORS			
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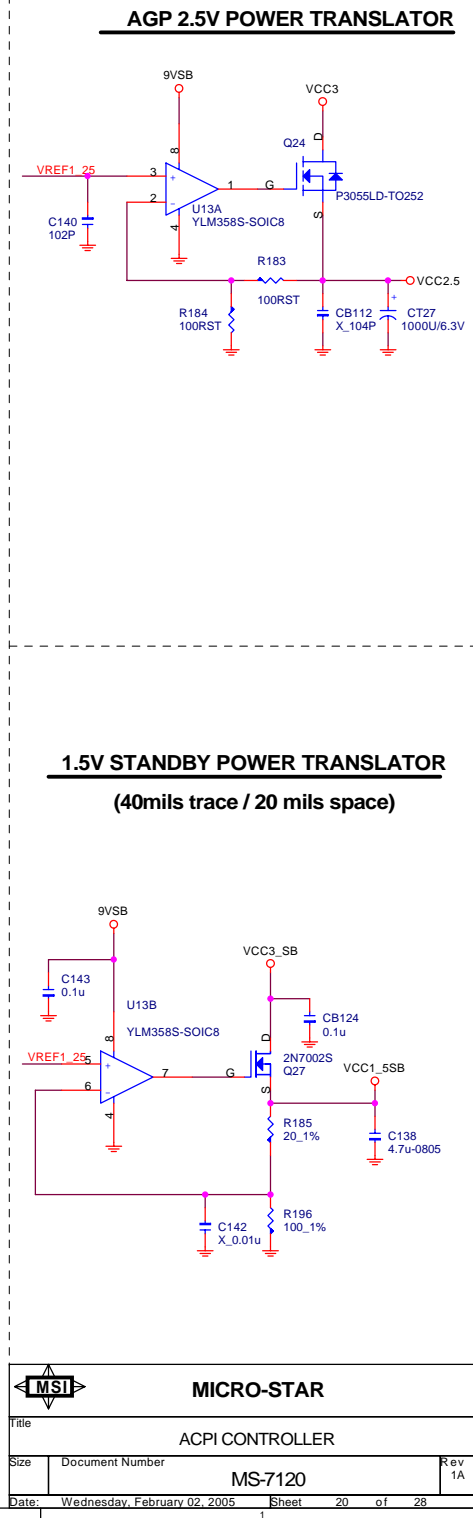
Power	S0	S3	S5
VCC3_SB	Main	Standby	Standby
VCC5_STR	Main	Standby	Standby
MEM_STR	Main	Standby	Standby

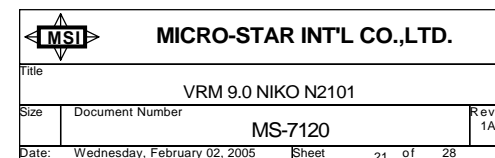
SEL0	5VUSB
H	2 MOSFET
L	1 MOSFET

**S50# pin function(Hi level = 5V)
same as 5VUSB(Hi level = 12V)
5VUSB USE 2 MOSFET

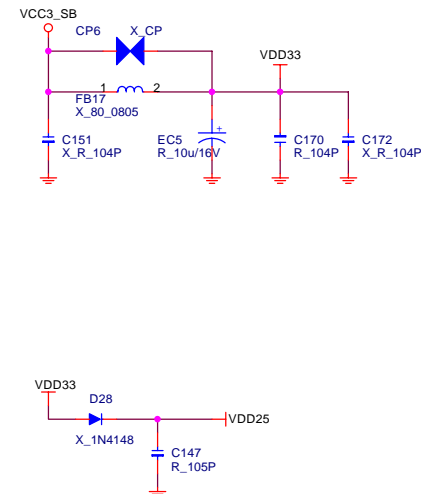
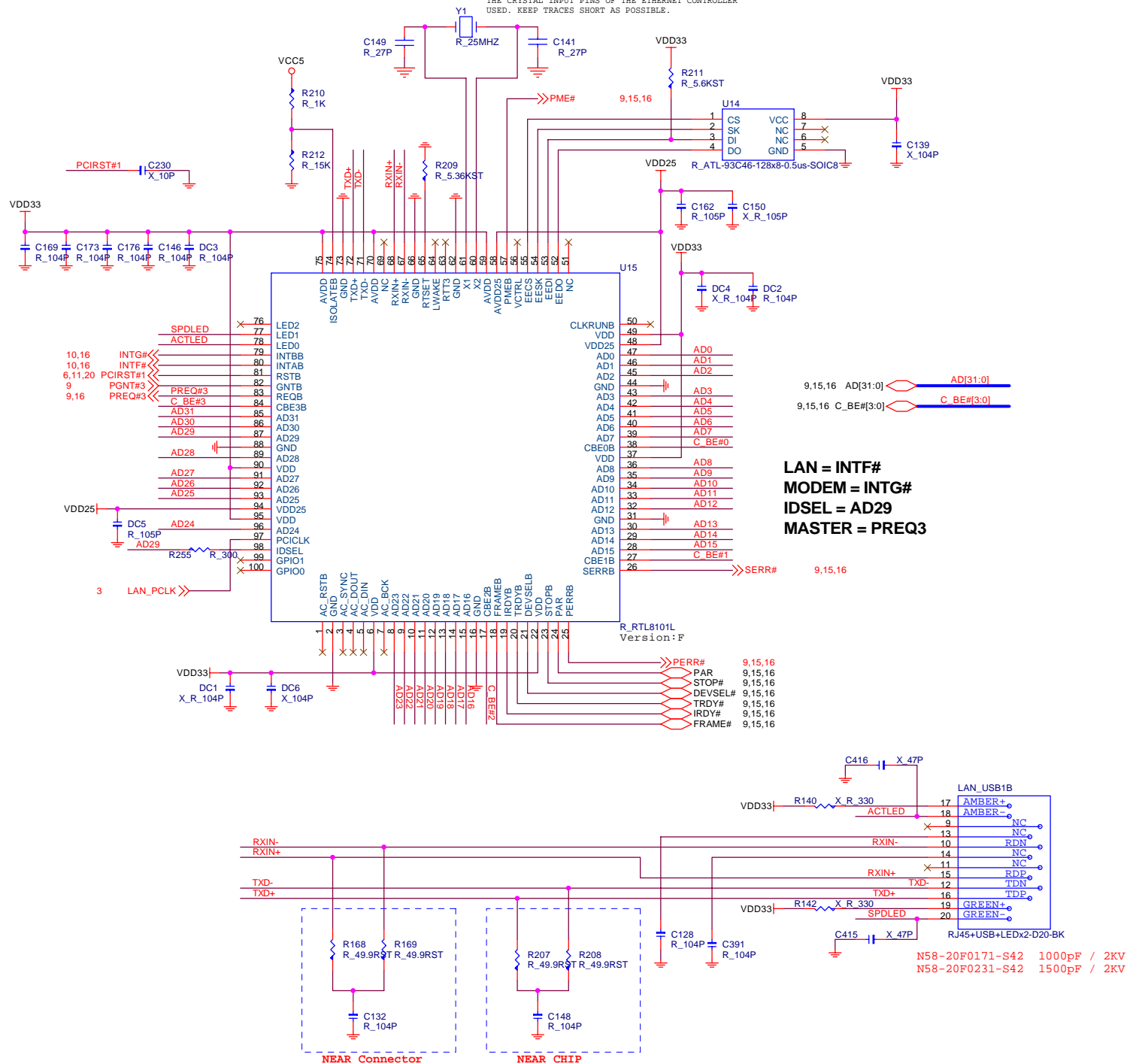


SEL1	VRAM	VRAM_2.5
H	3.3VDUAL	2.5V
TRI-STATE	3.3VSB	2.5V
L	3.3VSTR	1.25V





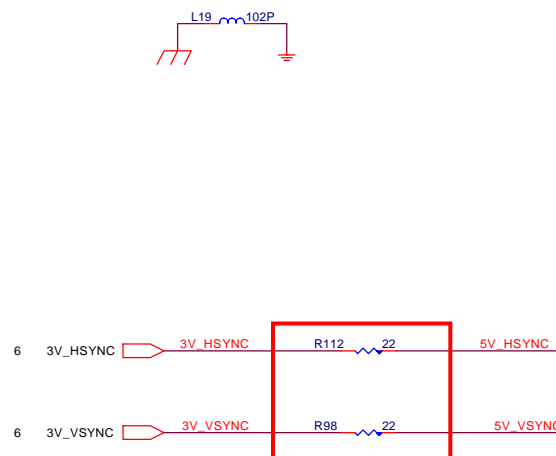
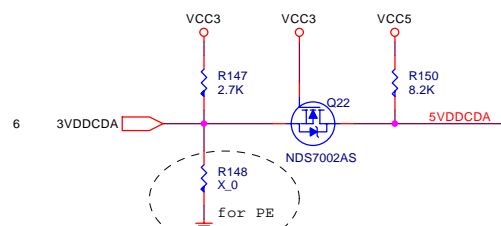
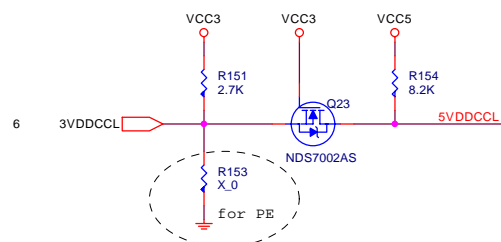
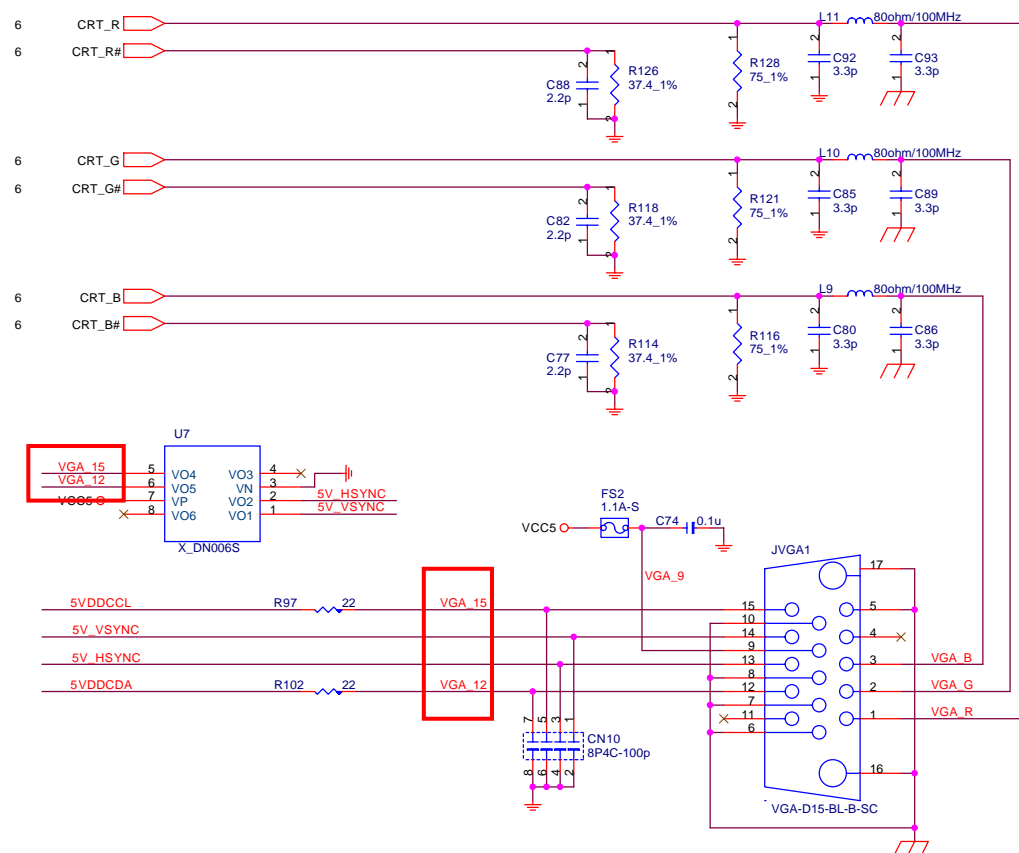
THIS DEVICE SHOULD BE PLACED AS CLOSE AS POSSIBLE TO THE CRYSTAL INPUT PINS OF THE ETHERNET CONTROLLER USED. KEEP TRACES SHORT AS POSSIBLE.



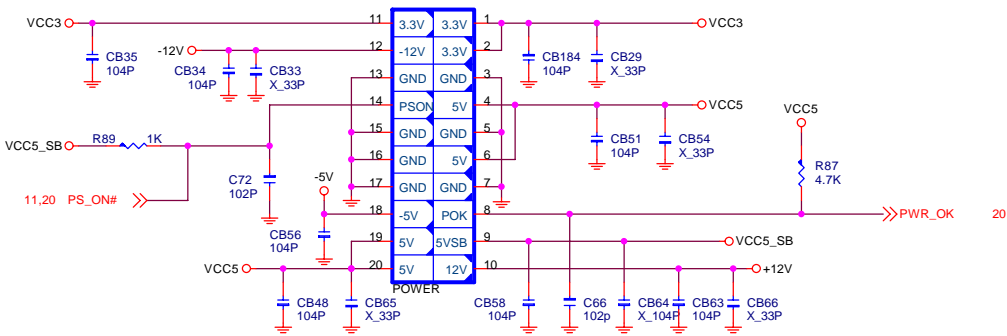
MICRO-STAR

Title			LAN REALTEK 8101L
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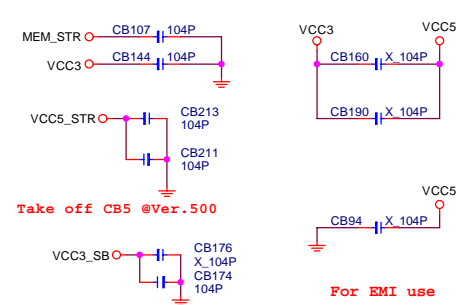
Video Connector



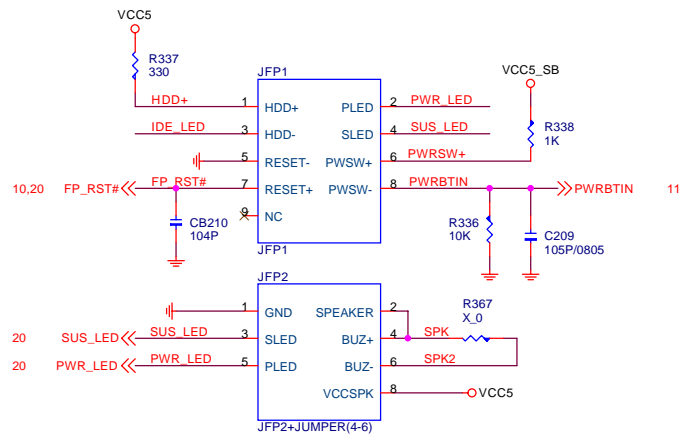
ATX CONNECTOR



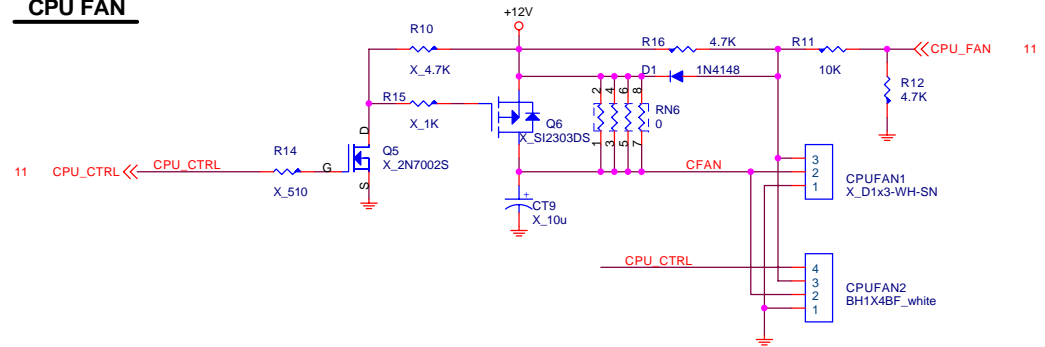
REGULATORS OUTPUT DECOUPLING CAPACITORS



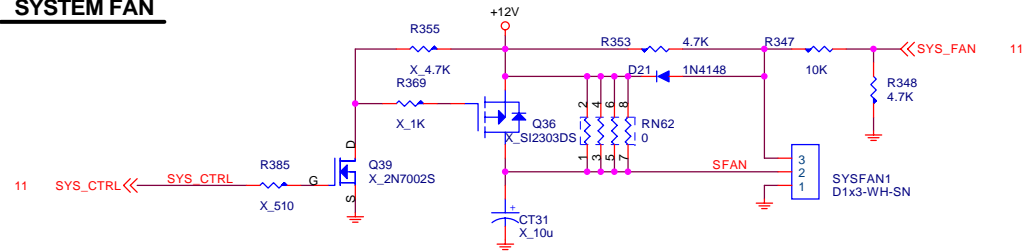
Intel Front Panel



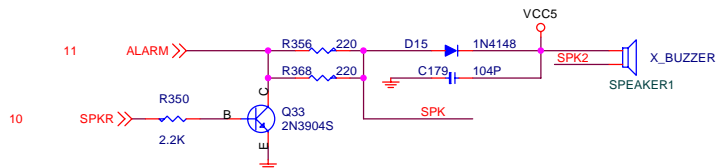
CPU FAN



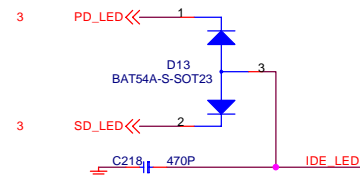
SYSTEM FAN




BUZZER



IDE LED



				MICRO-STAR			
Title							
Front Panel & ATX Connector & FAN							
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		MS-7120					
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